

# FPGA Implementation of Reversible Adder/Subtractor

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**Abstract** - This work presents the new design of the reversible adder/subtractor circuit. The proposed design of reversible adder/subtractor is compared to the existing counterpart in terms of design constraints such as the total number of reversible gates, no. of constant inputs and quantum cost. The delay and power of the proposed reversible adder/subtractor circuit were calculated, compared with existing reversible and conventional adder/subtractors.

**Keywords:** Reversible Adder/Subtractor, Reversible gates

## I. INTRODUCTION

In the early 1960's researcher, R. Landauer stated that during conventional logic operations when each bit of information lost results in  $KT \ln 2$  joules of energy dissipation regardless of the underlying technology [1]. Where  $K$  = Boltzmann's constant and  $T$  = Temperature.

In 1973 C.H. Bennett proved that dissipation of  $KT \ln 2$  amount of heat energy can be minimized or even avoided if the logic operation is performed in a reversible manner [2]. During the reversible computation, the information is not lost and reversible circuits offer significant reduction of power consumption. [3-5].

An adder/subtractor is a digital combinational circuit which can perform dual operations addition as well as subtraction operation depending on the value of the Ctrl input. When Ctrl is connected to logic '0' then the circuit works as an adder and when Ctrl is connected to logic '1' then the circuit behaves as the subtractor. Adder/Subtractor circuit is used to design complex computational units like ALU, multipliers and dividers etc [6, 7].

The paper is consists of sections as follows Section II discuss the reversible logic basics. Section III provides Literature survey. Section IV explains the proposed design. Section V shows simulation results and comparison. Section VI gives the conclusion.

## II. REVERSIBLE LOGIC BASICS

A Gate is said to be reversible gate when it consists of identical inputs and outputs and also has one to one mapping between input and output vectors.

The following are the parameters which play a major role to design an optimized reversible logic circuit are gate count, ancilla inputs, garbage outputs and quantum cost. The

Number of reversible gates employed in the implementation of the reversible circuit known as Gate Count. Reversible gate inputs which are retained at a fixed value either 0 or 1 to obtained desired output. These inputs are called ancilla inputs. Garbage outputs are defined as reversible gate outputs which are not needed for further operations in the reversible circuit. Quantum cost refers to the number of primitive reversible gates (1x1 and 2x2) essential for the design of the reversible circuit [8].

### A. Double Feynman Gate

The Double Feynman gate (DFG) is a 3 inputs, 3 outputs (3x3) reversible logic gate with mapping of inputs (A, B, C) to outputs ( $W = A$ ,  $X = A \oplus B$ ,  $Y = A \oplus C$ ) as shown in Figure 1. The quantum cost of the DFG is two [9].

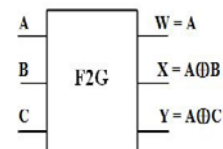


Fig. 1 Double Feynman Gate

### B. HNG

The HNG is a 4 inputs, 4 outputs (4x4) reversible logic gate with mapping of inputs (A,B,C,D) to outputs ( $W = A$ ,  $X = B$ ,  $Y = A \oplus B \oplus C$ ,  $Z = (A \oplus B)C \oplus AB \oplus D$ ) as shown in Figure 2. HNG can be work as a Full adder. The quantum cost of HNG is six [10].

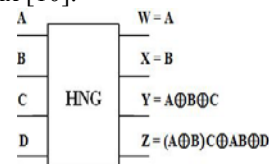


Fig. 2 HNG GATE

## III. EXISTING DESIGN

Rangaraju *et al.*, [11] proposed a reversible 8-bit parallel binary Adder/subtractor. In this design first, one bit adder/subtractor was implemented using two Peres and two Feynman gates. The two Peres gates are used as reversible Peres Full Adder Gate (PFAG) and two Feynman gates are used as an EXOR gate. This one-bit adder/subtractor design requires totally four reversible gates, utilizes one constant input, generates three garbage outputs and it has a quantum cost of ten. Next reversible 8-bit parallel Adder/subtractor is implemented by cascaded the one-bit full adder/subtractor and inputs are simultaneously applied. This 8-bit

adder/subtractor design requires totally 31 reversible gates and it has a quantum constant of 76. This design utilizes 8 constant inputs and generates 23 garbage outputs.

**IV. PROPOSED DESIGN**

The basic building blocks of the adder/subtractor circuit are the Full adder and EXOR gate. HNG is used as a full adder and a Feynman double gate is used to perform EXOR operations, which are needed in the adder/subtractor design. In the implementation of proposed reversible 16-bit adder/subtractor circuit, sixteen HNG and eight F2G reversible gates are utilized as shown in Figure 3. A inputs are directly applied to the HNG gates as one of the inputs,

whereas B inputs and control (Ctrl) are applied to the Feynman double gates. The ctrl terminal is connected to the Cin and also to one of the inputs of Feynman double gate. If logic '0' is applied to ctrl, the Feynman double gates behave as buffers whose outputs are an uncomplemented form of inputs and at this instant, the circuit performs an addition operation. If logic '1' is applied to the ctrl, the Feynman double gates act as inverters and its input data bits are complemented, now adder performs the addition operation of A data with the complemented form of B data along with a single bit logic '1' as Cin. This operation is identical to a subtraction operation using 2's complement [6].

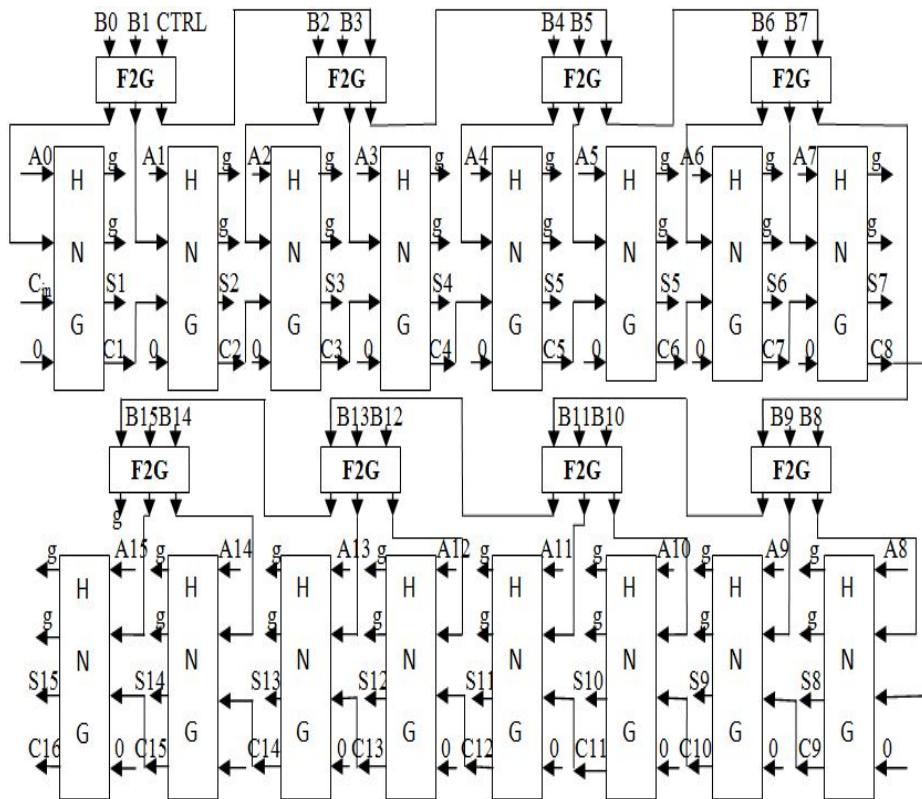


Fig. 3 Block diagram of Proposed 16-bit Reversible Adder/Subtractor

The proposed 16-bit adder/subtractor design requires totally 24 reversible gates and has a quantum cost of 112. The design utilizes 16 constant inputs and generates 33 garbage outputs. The gate count, garbage outputs, ancilla inputs and quantum cost for N bit reversible adder/subtractor are as follows [12].

- Reversible gates =  $N + (N / 2)$
- Garbage outputs =  $2N + 1$
- Ancilla inputs =  $N$
- Quantum cost =  $7N$

**V. RESULTS AND COMPARISON**

The proposed reversible adder/subtractor circuit was coded using Verilog Hardware Description Language. The

operation of a proposed reversible adder/subtractor design was tested using simulation process, synthesized and implemented using XC5VLX50T-1FF1136 FPGA in Xilinx 14.3. The experimental setup for FPGA implementation is as shown in Figure 4. Figure 5 shows the configuration of Proposed Reversible 16-bit adder/subtractor bit file to the FPGA. The simulation waveform of the proposed reversible 16-bit adder/subtractor as an adder is as shown in Figure 6. The Figure 7 to Figure 12 shows the Proposed Reversible 16-bit adder/subtractor as an adder whose outputs are in the decimal format for different hexadecimal input combinations. Figure 13 shows the simulation waveform of the proposed reversible 16-bit adder/subtractor as a subtractor. The Figure 14 to Figure 17 shows the Proposed Reversible 16-bit adder/subtractor as a subtractor whose outputs are in a decimal format for different hexadecimal

input combinations and also outputs appeared on Light Bar (as different colors). The RTL Schematic and Technology schematic of Proposed Reversible 16-bit adder/subtractor is as shown in Figures 18 and 19.



Fig. 4 Experimental setup

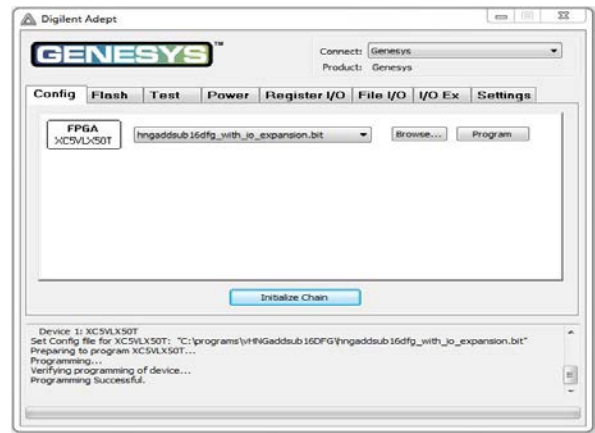


Fig. 5 Configuration of Proposed Reversible 16-bit Adder/Subtractor bit file to FPGA

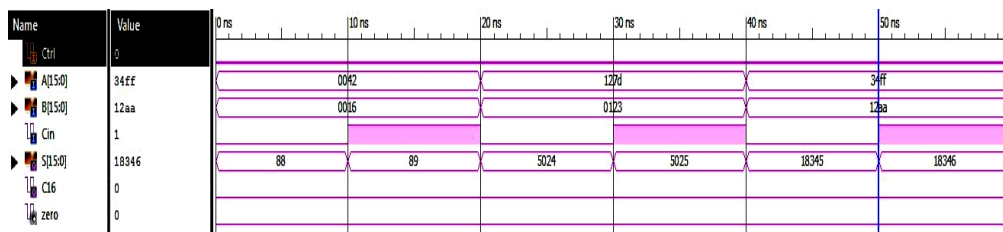


Fig. 6. Proposed Reversible 16-bit Adder/Subtractor simulation waveforms as an Adder

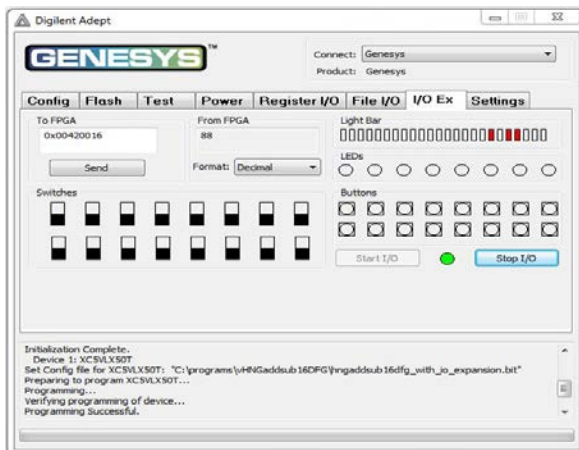


Fig. 7. Output of Proposed Reversible 16-bit Adder/Subtractor as an adder for input combinations A = 0042, B = 0016, Ctrl = 0 and Cin = 0

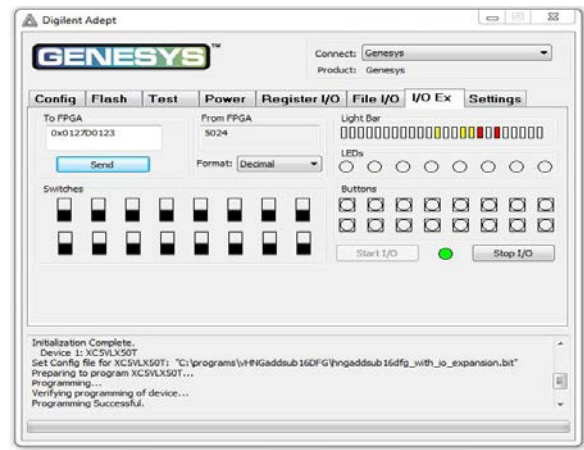


Fig. 9 Output of Proposed Reversible 16-bit Adder/Subtractor as an adder for input combinations A = 127D, B = 0123, Ctrl = 0 and Cin = 0

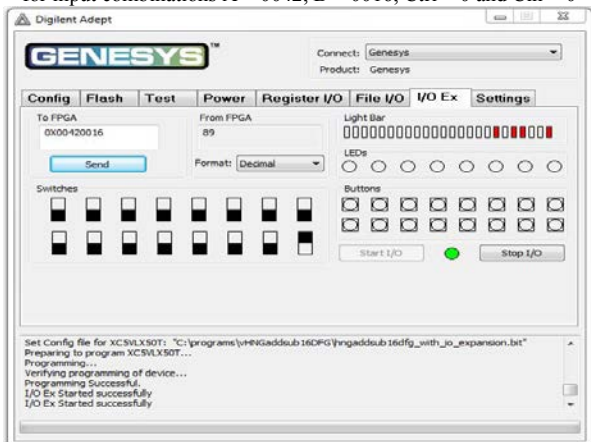


Fig. 8. Output of Proposed Reversible 16-bit Adder/Subtractor as an adder for input combinations A = 0042, B = 0016, Ctrl = 0 and Cin = 1

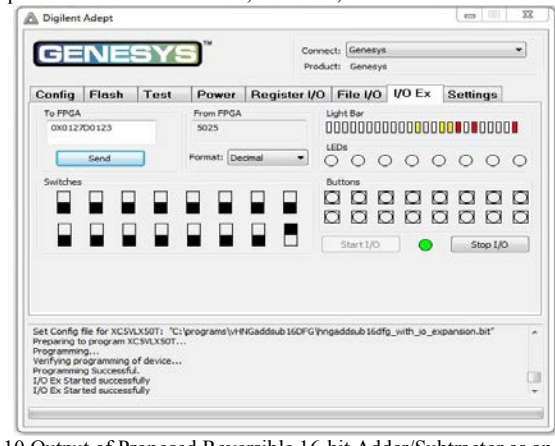


Fig. 10 Output of Proposed Reversible 16-bit Adder/Subtractor as an adder for input combinations A = 127D, B = 0123, Ctrl = 0 and Cin = 1.

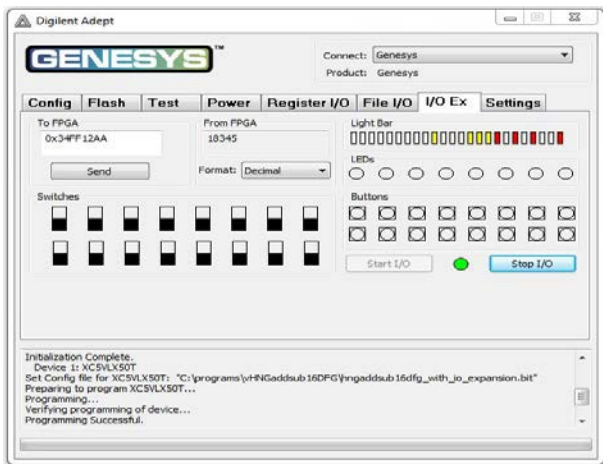


Fig. 11 Output of Proposed Reversible 16-bit Adder/Subtractor as an adder for input combinations A = 34FF, B = 12AA, Ctrl = 0 and Cin = 0

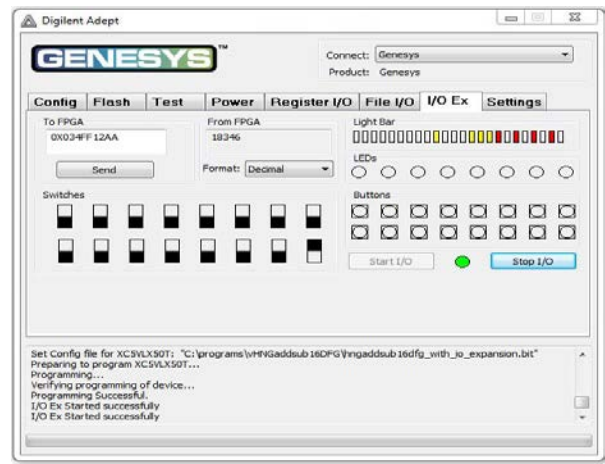


Fig. 12 Output of Proposed Reversible 16-bit adder/subtractor as an adder for input combinations A = 34FF, B = 12AA, Ctrl = 0 and Cin = 1

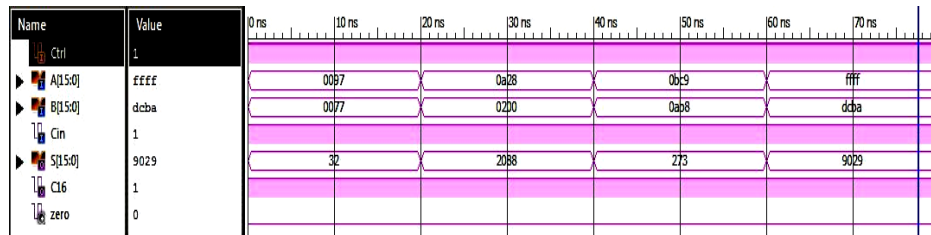


Fig. 13 Proposed Reversible 16-bit Adder/Subtractor simulation waveforms as a subtractor

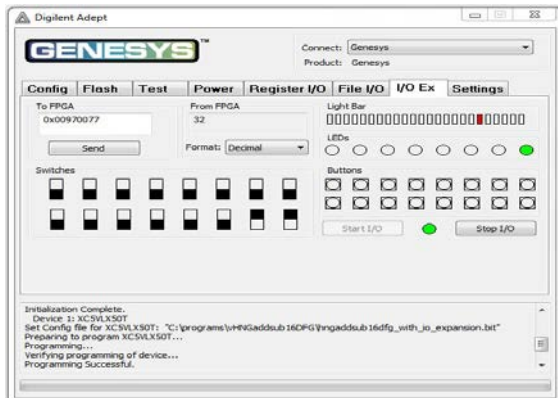


Fig. 14 Output of Proposed Reversible 16-bit Adder/Subtractor as a subtractor for input combinations A = 0097, B = 0077, Ctrl = 1 and Cin = 1

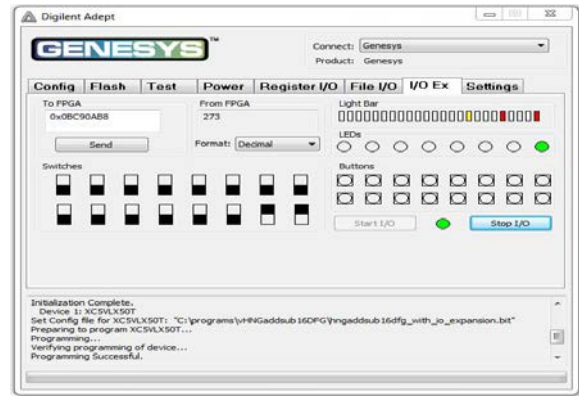


Fig. 16 Output of Proposed Reversible 16-bit Adder/Subtractor as a subtractor for input combinations A = 0B09, B = 0AB8, Ctrl = 1 and Cin = 1

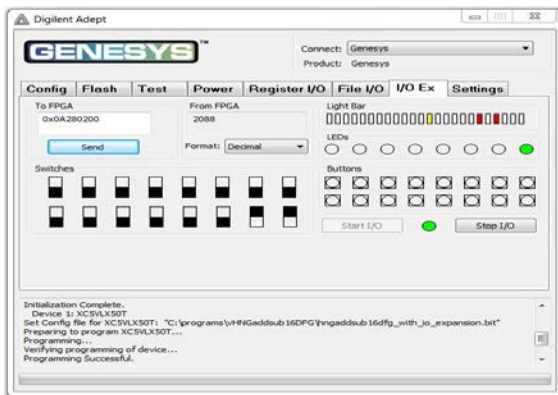


Fig. 15 Output of Proposed Reversible 16-bit Adder/Subtractor as a subtractor for input combinations A = 0A28, B = 0200, Ctrl = 1 and Cin = 1

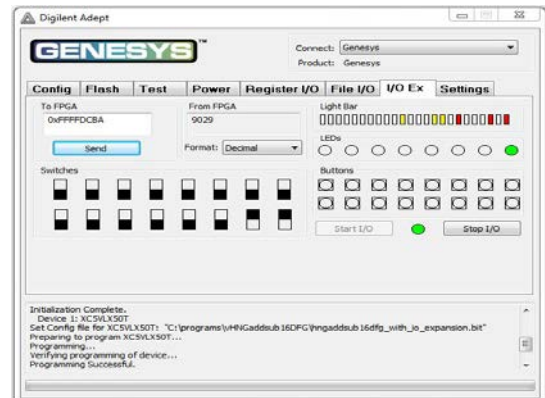


Fig. 17 Output of Proposed Reversible 16-bit adder/subtractor as a subtractor for input combinations A = FFFF, B = DCBA, Ctrl = 1 and Cin = 1

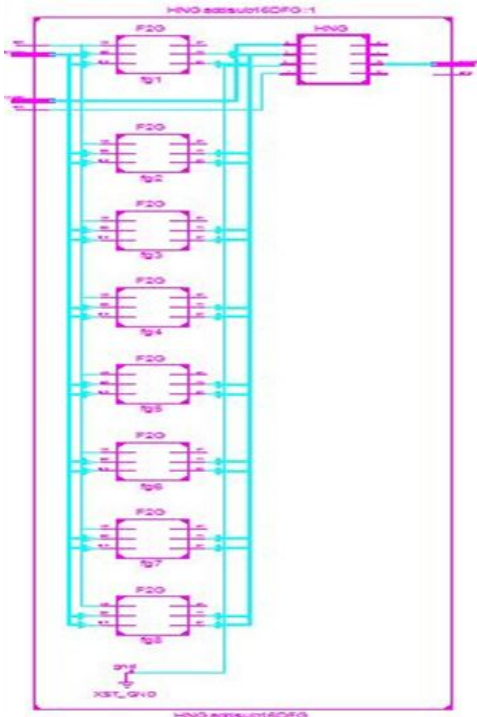


Fig. 18 RTL Schematic of Proposed Reversible 16- bit Adder/Subtractor

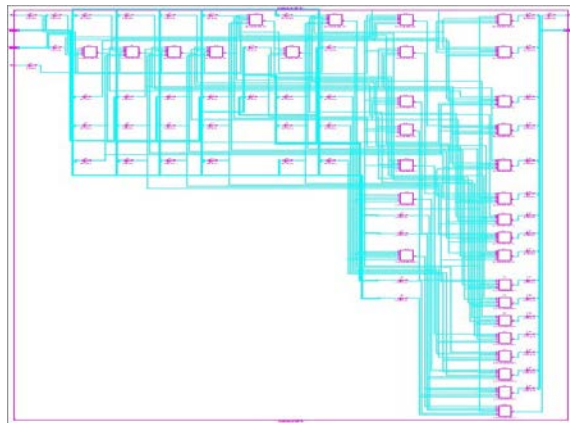


Fig. 19 Technology schematic of Proposed Reversible 16-bit Adder/Subtractor

Table I Shows the comparison between proposed and existing designs for 16-bit reversible adder/subtractor. The comparison is done on the design constraints such as reversible gates, garbage outputs, constant inputs and quantum cost.

TABLE I COMPARISON OF REVERSIBLE ADDER/SUBTRACTORS

16 bit Add/Sub Designs	Reversible Gates	Garbage outputs	Ancilla inputs	Quantum cost
Proposed design	24	33	16	112
Existing design [11]	63	47	16	156

Table II shows the comparison of delay and power between the proposed 16-bit reversible adder/subtractor design with the existing reversible design and irreversible logic design.

TABLE II COMPARISON BETWEEN REVERSIBLE AND CONVENTIONAL ADDER/SUBTRACTORS

16 bit Adder/Subtractor designs	Delay (ns)	Power ( $\mu$ w)
Proposed Reversible design	9.167	51
Existing Reversible design [11]	9.980	52
Conventional logic design	10.114	54

VI. CONCLUSION

This work presents an adder/subtractor design using reversible logic gates. From the Table 1 the proposed design for 16-bit reversible adder/subtractor has a 162.5% improvement in the number of reversible gates, 42.42% improvement of garbage outputs and 39.29% improvement of the quantum cost than existing counterpart. The delay and power of the proposed 16-bit reversible adder/subtractor design is compared with the other designs shown in Table 2 from this by estimation of the proposed design, it is demonstrated that the parameters such as delay and power consumption are reduced than the existing reversible and conventional logic designs and proved that the power consumption of the proposed and existing reversible logic designs are less than the conventional logic design.

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