Asian Journal of Electrical Sciences
ISSN: 2249-6297 (P) Vol.4 No.2, 2015, pp.10-15

DOI: https://doi.org/10.51983/ajes-2015.4.2.1950

Reordering of Test Vectors Using Weighting Factor Based on Average Power for Test Power Minimization

M.Vidhyia[1], K.Paramasivam[2], S.Elayaraja[3] and S.Bharathiraja[4]
[1]Assistant professor, Department of ECE, AVS Engineering College, Salem, Tamil Nadu, India
[2]Professor, Department of ECE, KSR College of engineering, Thiruchengode, Tamil Nadu, India
[3]Asst Professor(Sr.G), Department of Civil Engineering, PSG Institute of Technology & Applied Research, Coimbatore, Tamil Nadu, India
[3]Asst Professor, Department of Civil Engineering, Paavai college of Technology, Namakkal, Tamil Nadu, India
E-mail: [1]vidhyiaksm@gmail.com, [2]kp_sivam@yahoo.com, [3]elayaraja86@gmail.com , [4]Bharathiyes@gmail.com

***Abstract* - Power consumption is one of the biggest challenges in high performance VLSI design and testing. Low power VLSI circuits dissipate more power during testing when compared with that of normal operation. Dynamic power has been the dominant part of power dissipation in CMOS circuits; however, in future technologies the static portion of power dissipation will outreach the dynamic portion. The proposed approach is based on a reordering of test vectors in the test sequence to minimize the switching activity of the circuit using test application. In this paper weighted switching activity is derived based on the average power consumed in the logic gates during all possible event conditions. Since this weighted switching activity is based on the power, which gives more accurate results. The proposed algorithm is implemented and verified using ISCAS85 benchmark circuits. Power is estimated for the circuits using Tanner EDA tool. The results show that power is reduced significantly over the existing methods**

Keywords: **Weighted Switching Activity, Test Power, Reordering, Power dissipation, Power matrix**

I. INTRODUCTION

Power consumption has recently become a serious consideration in IC design and testing. Maximizing circuit speed and minimizing chip area used to be the only major concerns of VLSI designers. The growing size of VLSI circuits, high transistor density, and popularity of low power circuit and system design are making minimization of power dissipation an important issue in VLSI design. In recent years, power consumption of integrated circuits (ICs) has proved to be just as important of a concern. Thus, VLSI designs nowadays emerge as a tradeoff among three goals: minimum area, maximum speed, and minimum power dissipation. Excessive power dissipation causes overheating, which may lead to soft errors or permanent damage. It also limits battery life in portable equipment. Thus, there is a need to accurately estimate the power dissipation of an IC during the design phase. A lot of low power design techniques have been proposed at all levels of the design hierarchy. However, all these techniques focus on low power dissipation during system mode or standby mode, and do not consider the test mode. In test mode, the switching activity of all nodes often is several times higher than the activity during normal operation. Since heat or power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test can cause several problems. Excessive switching activity due to low correlation between consecutive test vectors can cause several problems. First, since heat dissipation in a CMOS circuit is proportional to switching activity, the circuit can be permanently damaged when the circuit experiences more switching activity [2, 3] during its operation. Second, it has been observed that metal migration or electro-migration causes the erosion of conductors and subsequent failure of circuits [2, 4]. Since temperature and current density are major factors that determine electro-migration rate, elevated temperature and current density caused by excessive switching activity during test application can severely influence the reliability of CUT. In this paper, a method is proposed to get accurate testing power by reordering the sequence of test vectors for minimum switching activity of the CUT. A set of test vectors are applied to the CUT during testing with the weighted factor. The order of application of vectors changes the total switching activity of the circuit. Lowest switching activity for a given order of test vectors is called minimum switching activity of the CUT. The order is called reordered test set. The test power obtained by applying the reordered test set is regarded as accurate test power. The power constraints that are usually considered during design are much lower than the power consumed during testing [3], thus causing severe reliability problems.

II. EXISTING METHODS

Many research works have tried to solve the power problem in high performance VLSI circuits. Test vector ordering with vector repetition has been presented as a method to reduce the average as well as the peak power dissipation of a circuit during testing. It also reduces the total switching activity by lowering the transition density at the circuit inputs. Experimental results validate that the proposed technique achieve considerable savings in energy and average power dissipation while reducing the length of the resulting test sequences compared to the original method [2]. Based

on re-ordering of the test-pair sequences, the switching activities of the circuit-under-test during test application can be minimized. Hamming distance between test-pair is defined to guide test-pair re-ordering. It minimizes power dissipation during test application without reducing delay fault coverage. The reordered test vector set with minimum hamming distance is used for testing the CUT to reduce the switching power. Hamming Distance approach is based on the concept that the internal switching activity is more or less depending on the hamming distance at the input of the circuit. This concept is not true for all the circuits and the switching activity is depending on the logic gates that are used to construct the circuit. In the work by Chakravarty and Dabholkar [5], the authors construct a complete directed graph in which each edge represents the number of transitions activated in circuit after application of the vector pair. The authors use a greedy algorithm to find a Hamiltonian path of minimum cost in the graph.

A scheme is proposed by Chattopadhyay and Choudhary [2] that uses a genetic algorithm based approach for reducing the hamming distance between consecutive patterns in the test set. As the hamming distance reduces, the switching activity in the circuit is also expected to reduce. In paper [9] Chattopadhyay and Choudhary use a genetic algorithm based approach for reducing the hamming distance between consecutive patterns in the test set. As the hamming distance reduces, the switching activity in the circuit is also expected to reduce. Also Girard et al.[2] propose using the Hamming distance between test vectors rather than the number of transitions in the circuit to evaluate the switching activity produced in the CUT by a given input test pair. Using the Hamming distance makes it possible to apply test vector reordering to large VLSI designs. Hamming distance method may not be accurate all the times, the bit change at the input of the circuit may or may not reduce the switching activity of the circuit. Reducing the hamming distance will not assure the power optimization. To overcome the difficulty, the actual switching activity is considered for reordering the test vectors.

III. BACK GROUND AND RELATED WORK

A. Energy and Power Modeling

Power dissipation is an important issue in both the design and test of VLSI circuits. Power consumption in CMOS circuits can be static or dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply which contributes very slightly in the overall power dissipation. The total leakage current in logic gates includes two components, namely, sub threshold and gate leakage. Dynamic power consists of switching power and short circuit power. Short circuit current flows during the time when both transistors are in ON state. It depends on the rise or fall times of the input waveform. It also depends on the load output capacitance. Decreases for larger output load capacitance. The peak short circuit current occurs at the time when the transistor switching off goes from linear to saturation region. Switching power results from the activity of a circuit in changing its states due to the charging and discharging of the effective capacitive loads. Dynamic power significantly contributes to total power dissipation.

Three parameters are important for evaluating the power properties of a CUT during testing.

1. The consumed energy directly corresponds to the switching activity generated in the circuit during test application, and has impact on the battery lifetime during remote testing.
2. The average power consumption is given by the ratio between the energy and the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption.
3. The peak power consumption corresponds to the highest switching activity generated in the CUT during one lock cycle. If the peak power exceeds certain limits, the correct functioning of the circuit is no longer guaranteed. For CMOS circuits, dynamic power is the dominant source of power consumption, which is consumed when nodes switch from 0 to 1 or from 1 to 0.

The energy consumed at node *i* per switching is ½Ci V^2_{DD} where Ci is the equivalent output capacitance and V_{DD} the power supply voltage [8]. Hence, a good approximation of the energy consumed in a period is ½Cisi V^2_{DD} where si is the number of switching during the period. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, and in a first approximation, capacitance Ci is assumed to be proportional to the fan-out of the node Fi [9]. Therefore, an estimation of the consumed energy Ei at node i is

$$Ei = ½.si.Fi.co. V^2_{DD}$$

where co is the minimum output load capacitance. According to this expression, the estimation of the energy consumption at the logic level requires the calculation of the fan-out Fi and the number of switching on node i, si. The fan-out of the nodes is defined by circuit topology, and the switching can be estimated by a logic simulator. The product si.Fi is named Weighted Switching Activity (WSA) of node i and is used as a metric for the energy consumption at that node, since it is the only variable part in the energy consumed during test application [7]. The WSA generated in the circuit after application of a pair of successive vectors TPk = (Vk-1, Vk) can then be expressed by:

$$WSA (TP_k) = \sum s (i, k).Fi$$

where i ranges all the nodes of the circuit and s(i,k) is the number of switching provoked by TP_k at node i. Consider now a pseudo-random test sequence TS of length L, where L is the test length required to achieve the targeted fault

coverage, the total WSA in the circuit during application of the complete test sequence is :

$$WSA_{TS} = \sum_{TPK} \sum_{i} s(i, k).Fi$$

IV. PROBLEM FORMULATION

The power dissipation during testing [3] is minimized by reducing the number of transitions in the circuit. Usually test vectors are in random and hence it is necessary to rearrange the order of occurrence of test vectors so that minimum switching activity between successive test vectors is obtained. The problem of minimizing switching power is solved by graph theory using Hamiltonian path [14] technique. Graph G (V, E) is defined with V nodes and E edges. The problem is formulated by considering the test vector as node and switching activity between them as edge cost of the graph. The graph considered here is complete graph whose all the nodes are connected each other with edges. Adjacency matrix for the graph is represented by average power weighting matrix APWF [ ] [ ] of order n x n. The matrix element APWF[i][j] represents weighting factor based on average power in the CUT when j^{th} test vector is applied after i^{th} test vector. In this graph, the Hamiltonian path is a path connected by all nodes with minimum total edge cost. Reordering algorithm is used to construct the Hamiltonian path, which is resultant reordered test vector set with minimum average power in CUT [8]. Hence this path offers reduced power dissipation in the CUT during testing [1]. Heuristic approach is used in the algorithm to find more suboptimal sequences. The more suboptimal solutions can be obtained when two or more values of APWF matrix APWF [ ] [ ] are identical. These solutions are called heuristic based sub-optimal solutions. The reordering algorithm used to minimize the average power during testing is given as follows.

A. Reordering Algorithm

The various parameters used in the algorithms are as follows: $t_1, t_2, \ldots t_n$ be n test vectors with m bits each. T={1,2,… k … n} where k represents k position in the vector set generated by ATPG. R is a set to store ordered test vector sequence.
Q is a set to store T-R.

Step1: Select an element APWF $[x_{min}][y_{min}]$ in the power matrix such that which is smallest value in the matrix. Add x_{min}, y_{min} to R; Q ← T-R; x ← y_{min}.
Step2: Select a test vector y_{min} such that APWF$[x][y_{min}]$ is minimum in the array.
Step3: Add y_{min} to R; Q ← T-R; x ← y_{min}.
Step4: Repeat the above two steps till Q becomes empty. This algorithm is applied for combinational benchmark circuits ISCAS85

V. PROPOSED METHOD

In this proposed method weighting factors are evaluated using average power dissipation during every gate transitions. The existing methods used hamming distance, switching activity and weighted switching activity based on fan-outs for reordering of test vectors. In weighted switching activity method each and every gate transitions are estimated to get approximate power. Though event occurs, depends up on the logic of the circuit switching activity may or may not occur in the particular gate. Hence, mere switching activity will not approximate the dynamic power precisely. Hence, power based weighting factor will give more precise solution for reordering of test vector. Like, function based distance reordering, switching activity based reordering, and power dissipation based reordering method gives better results than the predecessors. Also it includes static and dynamic power. But the draw back is the time complexity to evaluate power for all possible pair of test vectors. So in order to overcome the time complexity problem and to approximate the power accurately, the weighting factor based on average power will give better solution.

In this proposed method, average power for all possible initial and final conditions are evaluated for all logic gates such as AND, OR, NAND, NOR, XOR, XNOR, NOT are determined by implementing in Tanner EDA tool. Initial inputs to basic gates such as AND as A = 0, B = 0 are considered. When there is a transition from 0 0 to 1 0, the output is 0 for which average power consumed is determined as 89µW. While transition of inputs from 0 0 to 0 1, the output is same as 0 and the average power consumed for this transition is 342µW. Observing the above two conditions, it is understood that average power produced is with large difference though the output is same. Weighting factors to be designed based on the power dissipation and from the average power weighting factors are derived. Dynamic power is approximated by the weighting factor. Test vectors are reordered based on weighting factors for minimizing test power in combinational circuits. Instead of adding 1 these weighting factor for each logic gate is added.
Weighting factor can be calculated by using the following formula

Weighting factor for transition = Average power during transition / Minimum average power. Powers with negligible values are not considered for calculating weighting factors.For example transition 1 1 to 1 0 consumes 963µW and the weighting factor is 963 / 45 = 24.All the possible transitions and their weighted factor for NAND gate are given in table I.

TABLE I WEIGHTING FACTOR FOR NAND GATE

Transitions at Inputs A,B		Output	Average Power	Weight in g Factor
From	To			
0 0	0 1	1	315µW	8
0 1	0 0	1	293µW	7
0 0	1 0	1	84µW	2
0 1	1 0	1	580µW	15
0 1	1 1	0	40µW	1
1 0	0 0	1	345µW	9
1 0	0 1	1	127µW	3
1 1	0 1	1	554µW	14
1 0	1 1	0	57µW	1
1 1	1 0	1	963µW	24
0 0	1 1	0	45µW	1
1 1	0 0	1	920µW	23

VI. RESULTS AND DISCUSSIONS

Illustration is made with simple ISCAS85 benchmark circuit C17 to show the effectiveness of the proposed algorithm. The test vector set for C17 circuit is shown in table 2. The test set consists of 6 vectors and are serially numbered from t1 to t6 as given in table II.

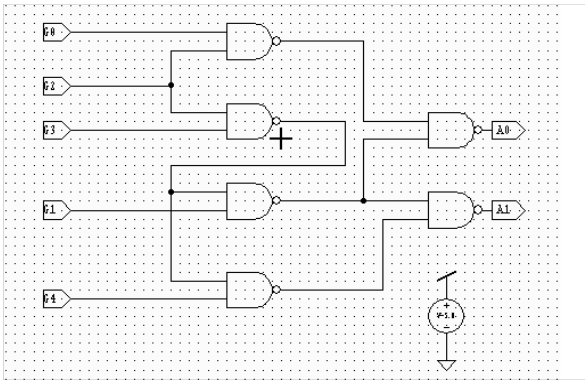

Fig. 1 C17 circuit

TABLE II TEST VECTOR SET FOR C17

No	Test Vector set
T1	11100
T2	11111
T3	00000
T4	01110
T5	01011
T6	10001

The C17 circuit is modeled in CMOS ML_0.25 (Technology) using T spice simulator of Tanner pro EDA tool and average power is calculated between all possible two test vectors set. Each circuit is implemented using VHDL to calculate the Average Power Weighting Factor matrix (APWF). The logic of the benchmark circuits are realized in VHDL. The counter is defined in the VHDL code for every signal of the circuit and incremented by the weighting factor of the basic gates for every event. Finally all the counters are added to find the total switching activity in the circuit. For c17 circuit the above reordering algorithm is applied and the following waveform shown in figure 2 is the evaluation of APWF matrix. Circuits are modeled in Tspice of Tanner pro EDA tool to evaluate the power dissipation. Experimental results show that a significant reduction in Peak power is achieved when reordered test vectors with the weighting factors are used for testing.

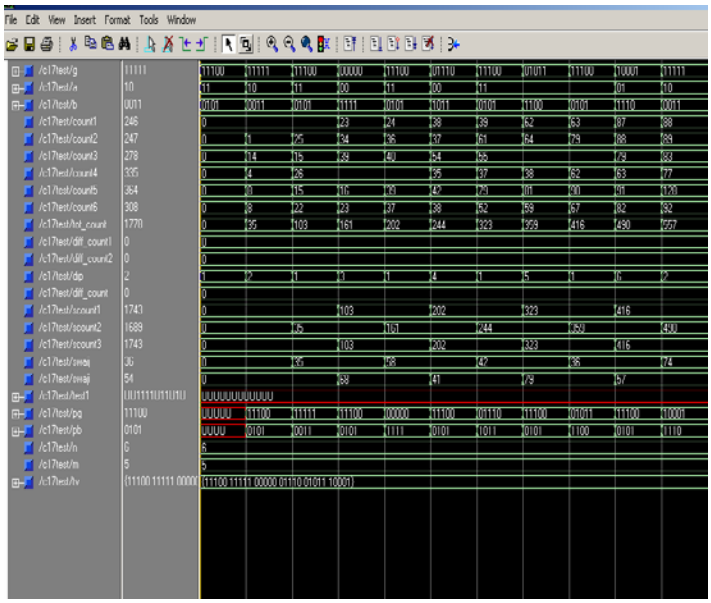

Fig. 2 C17 circuit waveform is evaluation of APWF matrix

$$APWF = \begin{pmatrix} 0 & 35 & 58 & 42 & 36 & 74 \\ 68 & 0 & 91 & 22 & 78 & 95 \\ 41 & 70 & 0 & 60 & 57 & 27 \\ 79 & 23 & 54 & 0 & 78 & 93 \\ 57 & 43 & 57 & 80 & 0 & 36 \\ 54 & 67 & 34 & 83 & 51 & 0 \end{pmatrix}$$

Using the above APWF matrix in the reordering algorithm, the sub optimal solutions are generated. From the table I I , experimental results show that the peak power is reduced compared to the existing method.

TABLE III C17 CIRCUIT

METHODS	AVERAGE POWER		PEAK POWER	
	UNORDERED	REORDERED	UNORDERED	REORDERED
Switching Activity Based	15.1mW	6.42mW	30.17W	14.73W
Hamming Distance	10.3mW	6.4mW		
Power based	10.3mW	6.4mW		
% of improvement	58%		51%	
Proposed method Power based				
% of improvement	58%		63%	

VII.CONCLUSION

In VLSI design process, power dissipation during testing is major concern. In this project a novel method is proposed for test power minimization to get accurate results. Since the total power dissipation is higher due to switching activity, the proposed algorithm is to reduce the switching activity by reordering the test vectors by considering the weighting factor evaluated based on average power in the logic gates. This method is implemented in ISCAS85 benchmark circuits using tanner pro EDA tool to evaluate the average power. Results show that an improvement is achieved for peak power in proposed method over the unordered test set.

REFERENCES

[1] P.Girard, C. Landrault, S. Pravossoudovitch and D. Severac, "Reducing Power Consumption during Test Application by Test Vector Ordering ", IEEE Int. Symp. on Circuits and Systems, CD-Rom proceedings, June 1998.

[2] M.Abramovici, M.A. Breuer and A.D. Friedman,"Digital Systems Testing and Testable Design", Computer Science Press, 1990.

[3] Fadi A. Aloul and Assim Sagahyroon , " Estimation of the Weighted Switching Activity in Combinational

[4] CMOS Circuits", American University of Sharjah, U.A.E

[5] P.Girard, L.Guiller, C. Landrault and S. Pravossoudovitch, "A Test Vector Ordering Technique for Switching Activity Reduction during Test Operation ", IEEE Great Lakes Symp. on VLSI, pp. 24-27, March 1999

[6] V. Dabholkar, S.Chakravarty I. Pomeranz and S.M. Reddy, "Techniques for Reducing Power Dissipation During Test Application in Full Scan circuits",IEEE Transactions on CAD, Vol. 17,N" 12, pp. 1325-1333,December 1998.

[7] P. Girad, L. Guiller, C. Landrault and S. Pravossoudovitch, "A test vector inhibiting technique for low energy BIST design," in Proc. VLSI Test Symp.,Apr 1999, pp. 407-412.

[8] S. Chattopadhyay and N. Choudhary, "Genetic Algorithm based Approach for Low Power Combinational circuit Testing" 16th IEEE International Conference on VLSI Design, January 4.8.2003, pp. 552-557.

[9] S. Chattopadhyay, "Reordering Test Pattern with Don't Cares for Minimizing Power Dissipation During Combinational Circuit Testing", Proc. Of Fourth International Conference on Information Technology, December 2001, pp. 260-264.

[10] P.Girard, L.Guiller, C. Landrault, S. Pravossoudovitch, J.Figueras, S.Manich, P. Teixeira and M. Santos, "Low Energy BIST Design: Impact of the LFSR TPG Parameters on the Weighted Switching Activity", IEEE Int. Symp. on Circuits and Systems, CD-ROM proceedings, June 1999.

[11] David Bryan, "The ISCAS '85 Benchmark Circuits and Net list Format" North Carolina State University, 1985.

[12] K.Paramasivam, K.Gunavathi, "Reordering Algorithm for Minimizing Test Power in VLSI Circuits", 12 February 2007

[13] Kuppusamy Paramasivam, and K.Gunavathi, "Switching Activity Based Method for Minimizing Testing Power in Digital Circuits"February2007.