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2nd Order Sigma Delta Modulator Design using Delta Sigma Toolbox

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***Abstract* - This paper discusses the block level design of 2nd order sigma delta using the Delta Sigma Toolbox and Simulink .An optimized modulator is designed with scaled coefficients, giving a low power, low frequency and high OSR modulator. The modulator presented has an OSR of 256, bandwidth of 200Hz, SNR of 100dB, SNDR of 96 dB, ENOB of 16 bits (approx.).The designed modulator is ideal for low power and low frequency applications, as in case of conversion of brain wave signals which are in the frequency range of 10-100Hz.This work provides the baseline for the design of the same modulator using switched capacitor in CMOS technology of 0.18µm TMSC CMOS technology with VDD of 1.8V.The coefficient values a, b, g, c are the ratios of capacitors in switched capacitor level design.**
***Keywords:* Sigma Delta, Delta sigma, Simulink, MATLAB, CMOS, ADC, EEG Sensor.**

I. INTRODUCTION

The increasing demand for audio devices for portable or autonomous apparatuses used in daily life continues to drive the need for highly power-efficient data converters with high resolution. Delta-sigma modulators (ΣΔ)are the preferred solution and the ones based on switched capacitor (SC) are optimal for low power medium conversion speed because of their accurate setting of zeros of the noise transfer function (NTF) and their insensitivity toward clock jitter and process Sigma delta (ΣΔ) analog-to-digital converters (ADCs) are generally utilized to achieve a high signal-to-noise ratio (SNR). The SNR of a ΣΔ ADC can be found using the conventional formula given in equation (1) and in decibels using equation (2), in which L represents the order of the ADC and N is the number of bits in the quantizer. To achieve the targeted SNR value, L, N, and oversampling ratio (OSR) values can be chosen as desired. Usually, the design is simpler when the ADC is 2nd order and N is 1, which leads to high OSR values. There arevarious methods of obtaining the desired transfer function, such as adding feedforward paths in the designs. Using feedforward paths in the ADC is a common method to cancel the effect of the input at the outputs ofthe integrators.[1] [2]

$$SNR = \frac{\frac{3}{2}(2L+1)}{\pi^{2L}} OSR^{2L+1} 2^{N-1} \quad (1)$$

$$SNR = 6.02M + 1.76 + 3.01(2L+1)log_2 OSR - 10log_{10}\left(\frac{\pi^{2L}}{2L+1}\right) \quad (2)$$

$$ENOB = \frac{SNR - 1.76}{6.02} \quad (3)$$

This paper explains the block level design of the Σ Δ modulators of 2nd order with a high OSR value using the Delta Sigma Toolbox and Simulink. This procedure forms the starting step in the circuit level design of Σ Δ modulators using CMOS technology. As the block level design in MATLAB is used to calculate the all-important modulator coefficients which serve the purpose of desired modulator response and constraints. The present work aims at showing the design of a sigma-delta modulator as part of an analog-to-digital converter (ADC) for low frequency and low power application used in digitizing the brain wave signal from an EEG headband sensor. Digitization of Brain waves requires high accuracy (more than 16 bits) or ENOB (Effective number of bits given by equation (3) and a bandwidth that range from 1Hz to 200Hz. Hence, the main focus of this work is to design a SD modulator that accomplish the application requirements considering the issues at each stage of the top-bottom design flow (from the system level to physical design). Following is the specification table of the modulator to be designed.[4]

TABLE I MODULATOR SPECIFICATIONS

Parameter	Value
SNR_{peak}	>96dB
BW	10-200Hz
OSR	256
Fs	100KHz
V_{DD}	1.8V
Modulator Order	2
Modulator Topology	Full Feed Forward
Domain	DT
ADC Levels	2
Topology	CIFF

II. SYSTEM LEVEL DESIGN

The paper focuses on the design and definition of the parameters of the Modulator blocks using the Delta Sigma toolbox and Simulink. The modulator coefficients are obtained and these values are optimal for providing maximum SNR and occupied the lowest area. Finally the overall 2nd order modulator were characterized and specified with these parameters and simulated as a block in Simulink.[3]

A. Delta Sigma Toolbox

Delta Sigma toolbox is an added tool in MATLAB environment for specific designing of ΣΔ based blocks. This toolbox is important for design and complete analysis of ΣΔ

modulators use in ΣΔ ADC and ΣΔ DAC structures. The design of the proposed ΣΔ modulators in some using the same toolbox and follows a specific set of steps.[5] [6]

The first step in the design of amodulator is the selection of the NTF. The modulator order, the number of quantization levels, and the choice of low pass. Band pass or quadrature modulation are all design parameters.The following MATLAB code is used to synthesize our proposed modulator and check the pole-zero and frequency response plots of the same. These plots can be used to estimate the number of quantization levels and the modulator order needed to achieve a particular OSR-SNR target. Once approximate values for these parameters have been selected, the designer can perform a detailed examination of the NTFs surrounding this point in the design space.[7]

```
Order = 2;OSR =256;Opt =2;
H_inf=1.5; f0=0;
H=synthesizeNTF (order, OSR, opt);
Subplot (2, 1,1); plotPZ (H);
Title ('Pole Zero Plot of NTF');
f=linspace (0,0.5,1000);z=exp(2i*pi*f);
Subplot (2, 1, 2); plot (f, dbv (evalTF (H,z)));
Title ('Frequency Response of NTF');
Xlabel('normalized frequency');ylabel('dB');
sigma_H=dbv(rmsGain (H,0,0.5/OSR));
```

Variable H is a complex variable that contains the synthesized modulator noise transfer function with the given specifications. Sigma_H contains the in band gain of the modulator which is equal to -70.0720 dB. The output plot is given in figure 1.[8]

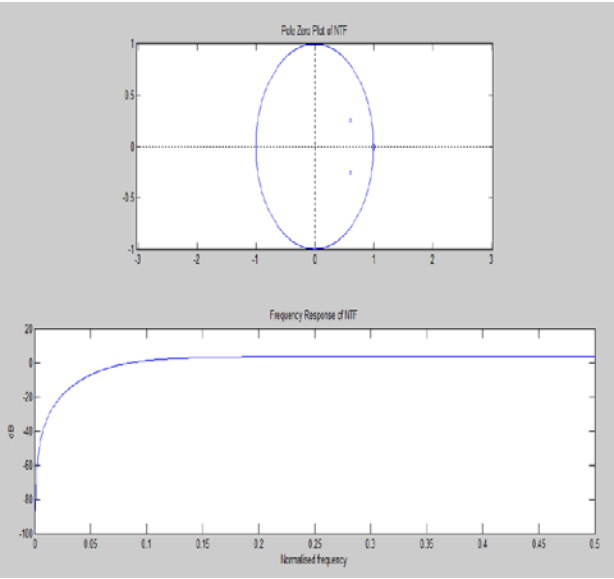

Fig. 1 Pole zero plot and Frequency Response(NTF)

Once an NTF is in hand, the designer can immediately begin to evaluate the modulator via simulation. The toolbox function simulateDSM computes the output of a modulator which realizes the desired NTF, assuming the STF is unity. Since the input-output behavior of an ideal SD modulator is determined solely by the NTF, the STF, the number of quantizer levels and the initial state, the behavior predicted by simulateDSM in terms of stable input range, tone performance and SNR is the same as it would be for any realization of the desired NTF [4]. Internal details of the loop filter are only relevant when one is concerned with coefficient errors, saturation of internal nodes and other non-ideal effects. The primary arguments to simulateDSM are the input sequence and the NTF. Secondary arguments include the number of quantizer levels (nlev), which defaults to 2, and the modulator's initial state (x0), which defaults to zero. A code fragment for simulating a 2-level low pass modulators and for plotting portions of its input and output waveforms is shown in Figure 2, along with the associated graphical output. The input signal was chosen as a half-scale sine wave in order to avoid overloading the modulator, and the frequency of the sine wave was chosen such that it would fall into one of the in-band frequency bins of an 8192-point FFT. The waveforms of Figure 2 provide an illustration of input of the modulator and its output.[9] [10]

```
Order=2;OSR=256;nLev =2opt=2;
H = synthesizeNTF(Order,OSR,opt);
Nfft=2^13;tone_bin=9;t=(0:Nfft-1);
u=0.5*sin(2*pi*tone_bin/Nfft*t);
v=simulateDSM (u,H,nLev);n=1:150;
stairs(t(n),u(n),' g');hold on;stairs(t(n),v(n),' b');
Title('Input Output Simulation of DSM');
Xlabel('Number of Sample'); Ylabel('Amplitude');
```

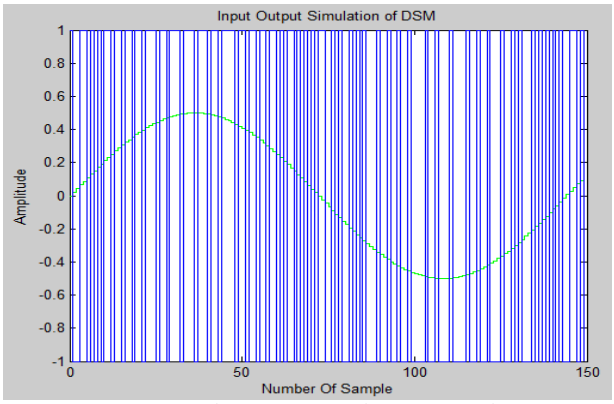

Fig. 2 SDM output from SD toolbox for given specifications.

As this figure shows, the only similarity between the input and output waveforms in the time domain is that when the input is positive, the output is usually either +1 or 0, and that when the input is negative, the output is usually either -1 or 0. However, when viewed from the frequency domain, the near-equivalence of the input and output (in the band of interest) becomes clearer. Figure 3 plots the *FFT* of a length-8192 output stream and superimposes the expected PSD.The code portion to view the frequency domain response is given under.[11]

```
Spec=fft (v)/(Nfft*(nLev-1)/2);
```

```
Snr=calculateSNR (spec (1: ceil (Nfft/(2*OSR))+1),tone_bin);
NBW=1/Nfft;f=linspace (0,0.5,(Nfft/2)+1);
Sqq=4*(evalTF(H,exp(2i*pi*f))/(nLev-1).^2/3);
Plot(f, dbv(spec(1 :( Nfft/2)+1)));
Title('SNR PLOT of DSM');
Xlabel ('normalized frequency');ylabel('dBFS');
Hold on;plot(f,dbv(Sqq*NBW),'m','Linewidth',1);
```

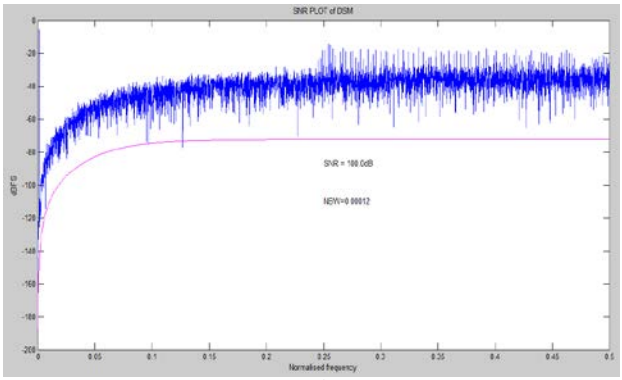

Fig. 3 SNR plot of the modulator.

It is clearly seen that the SNR is > 100dB and SNDR is > 90dB.this gives the ENOB of approximately 16 bits. The value of peak SNR for a given set of inputs is more reliable way of obtaining the parameters. For that the given set of code comes handy. [4]

```
OSR = 256;order=2;opt=2;
H = synthesizeNTF (order,OSR,opt);
[Snr_pred, amp] = predictSNR(H,OSR);
[Snr, amp] = simulateSNR (H,OSR);
[pk_snr,pk_amp] = peakSNR (Snr, amp);
Plot(amp,snr_pred,'b', amp,snr,'r'); Grid on;
FigureMagic([-120 0], 10, 2,[0 120], 10, 1);
Xlabel ('Input Level, dB'); ylabel ('SNR dB');
s=sprintf('peak SNR = %4.1fdB\n',pk_snr);
Text(-65, 15,s);
```

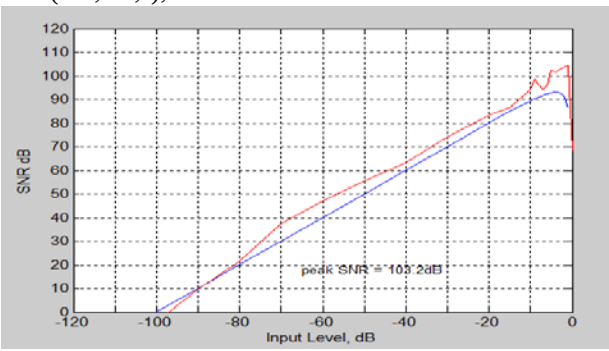

Fig. 4 Peak SNR.

Once the designer is satisfied with the performance of the NTF, the next step is to realize that NTF with a particular modulator structure. Although the toolbox can represent just about any modulator structure, code for converting an NTF into coefficients is currently only available for four of the most popular structures. These four structures are the feedback (FE) and feedforward (FF) versions of loop filters containing either only delaying integrators or alternately delaying and non-delaying integrators loop filters of the former are of termed as cascade-of-integrator (CI) filters, whereas the latter are termed cascade-of-resonator (CR) filters' and thus the four supported topologies which are fully supported by the toolbox bear the abbreviations CIFB, CIFF, CRFB and CRFF.As we have already discussed the type we will be designing is CIFF.The STF is calculated by the toolbox function calculateTF from a generic loop-filter description (the ABCD matrix), which is computed by the stuffABCD function from the topology-specific a, g, band c coefficients. The coefficients returned by realizeNTF are those of an *unsealed* modulator, i.e. a modulator whose internal states occupy an unspecified range. In order to restrict the state range to known (and practical) values, *dynamic-range scaling* must beperformed. Dynamic-range scaling can be applied to any linear system on a state by-state basis as depicted in Fig. 8.9, which shows how an internal state is scaled down by a factor *k* simply by reducing all incoming branches to that state by a factor of *k*, and by making up for the attenuation so introduced by multiplying all outgoingbranches by the same factor *k*.The toolbox function scaleABCD uses simulations to determine the required scalingfactors for each state of a delta-sigma modulator. The modulator is simulatedwith inputs of various amplitudes in order to determine the maximum stable inputamplitude (umax) as well as the maximum value that each state achieves for inputamplitudes up to umax. The ABCD matrix of the modulator is then subjected to dynamic range scaling so that the maximum value of each state equals the specified limit (xlim, which defaults to 1). The toolbox function mapABCD then translates the scaled ABCD matrix back into the coefficients for the chosen topology. The code segment below gives the complete realization of desired modulator.[9]

```
Order=2;OSR=256;nLev =2;opt=2;
Xlim=0.9;f=0;H = synthesizeNTF (order,OSR,opt);
Form = 'CIFF';
[a,g,b,c] = realizeNTF (H,Form);
ABCD = stuffABCD (a,g,b,c,Form);
[ABCDs,umax]=scaleABCD (ABCD,nLev,f,Xlim);
mapABCD (ABCDs,form); %scaled ABCD matrix
[Ha, Ga] =calculateTF (ABCD);
f =linspace (0,0.5,1000);z =exp (2i*pi*f);
MagHa =dbv(evalTF(Ha,z));
MagGa = dbv(evalTF(Ga,z));
Plot(f,magHa, 'b', f,magGa, 'm', ‘Linewidth’,1)
```

The coefficients of the modulator are given as:
a = [a_1=0.7749 a_2=0.2164]
b = [b_1=1 b_2=0 b_3=1]
c = [c_1=1 c_2=1]
g = [0]
After dynamic range scaling the parameters with, maximum input as 0.9 full scale input, we obtain new coefficient as:[3]
a1 = [$a1_1$=1.1007 $a1_2$=5.3789]
b1 = [$b1_1$=0.704 $b1_2$=0 $b1_3$=1]
c1 = [$c1_1$=0.704 $c1_2$=0.0571]

g1 = [0]

The NTF is obtained as:

$$\frac{(z-a-1)^2}{(z^2-1.225z+0.4415)}$$

The maximum stable input is given as umax=0.9667 of full scale input. [7]

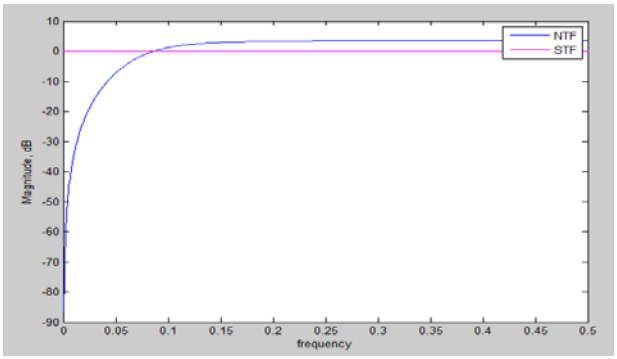

Fig. 5 NTF and STF of proposed modulator

III. SIMULINK MODELS

In order to predict the system level behavior and help in the design procedure, two Simulink models were elaborated: unscaled and quantized modulators. The former consists of discrete integrators, coefficients and an ideal quantizer in the form of a sig function block Despite the fact that this is an ideal model, the saturation voltage of the integrator was set at the standard supply voltage of the technology (VDD = 1.8V) to assure that the output of each integrator does not exceed the maximum allowed voltage. This restriction is the key of the model since it reduces the combinations of coefficients that attain the SNR specified for a given input amplitude. Thus, the model was basically used to iterate the coefficients until the desired response was reached. On the other hand, the output spectrum helps to estimate an accurate quantization noise power in the signal band, since the hand-calculation values are not accurate due to the 1-bit quantizer.[10] [5]

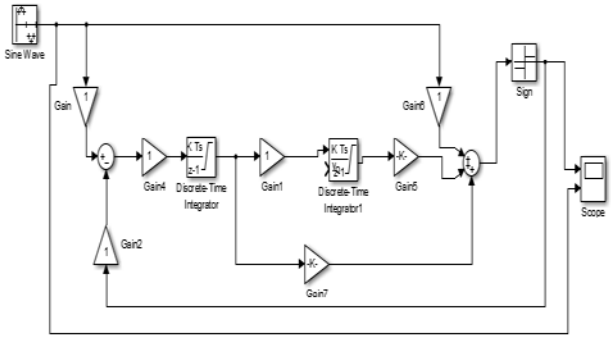

Fig. 6 Unscaled Modulator.

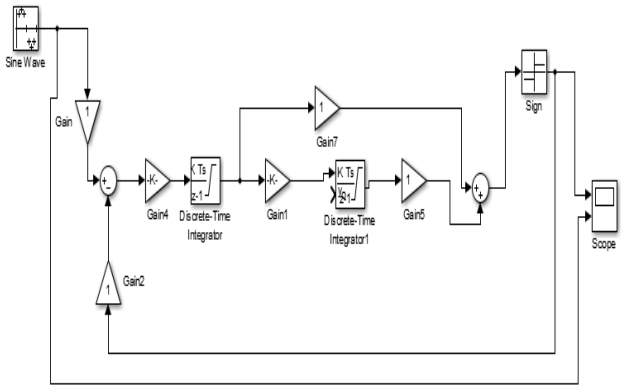

Fig. 7 Proposed unscaled Modulator.

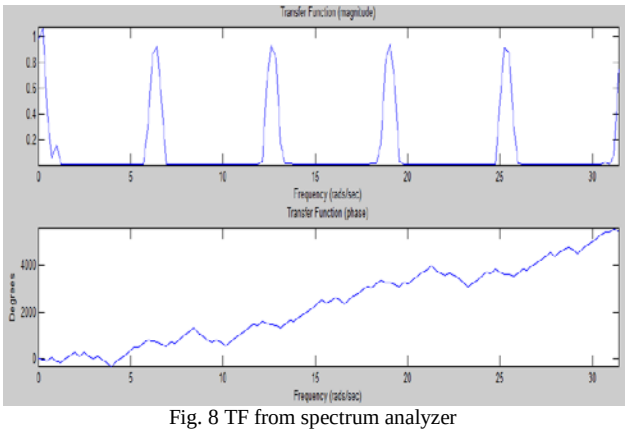

Fig. 8 TF from spectrum analyzer

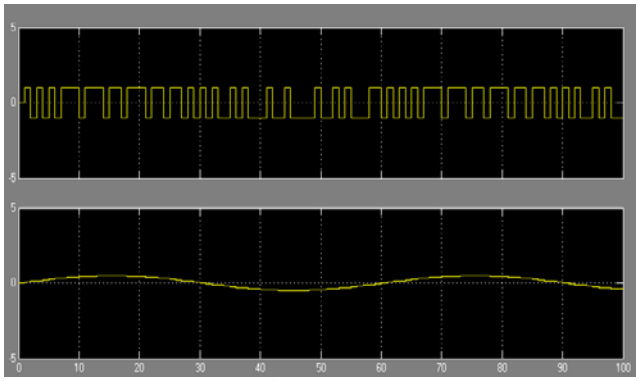

Fig. 9 Output of unscaled modulator.

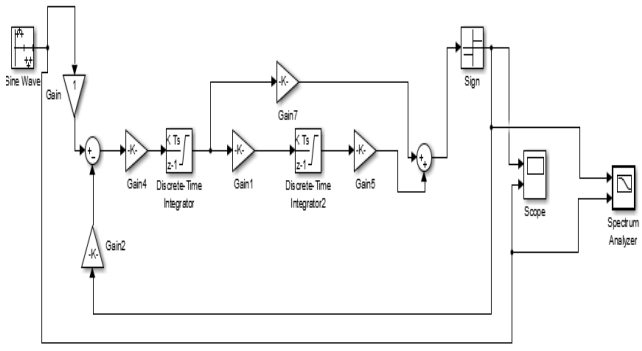

Fig. 10 Proposed scaled

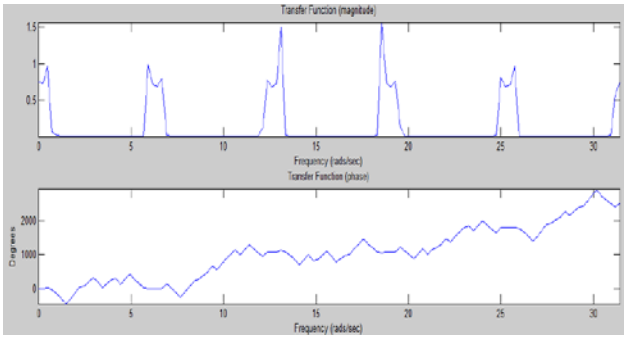

Fig. 11 Scaled TF

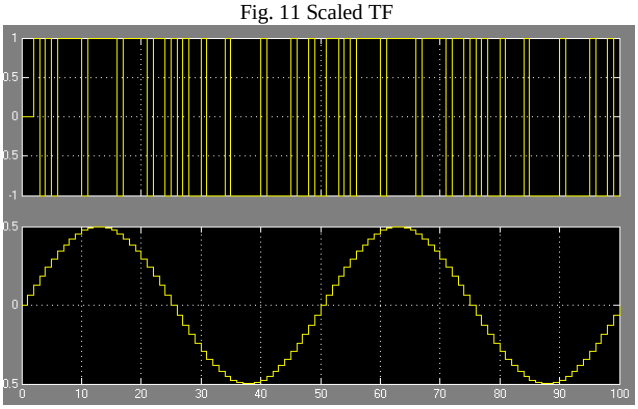
Fig. 12 Proposed Scaled Output

IV. CONCLUSION

In this paper the block level design of 2nd order sigma delta modulator using the Delta Sigma Toolbox and Simulink was presented. The design was modified to optimize the modulator coefficients. The a low power, low frequency and high OSR modulator was designed with an OSR of 256,Bandwidth of 200Hz,SNR of 100dB,SNDR of 96 dB, ENOB of 16 bits(approx..).The designed modulator is ideal for low power and low frequency applications, as in case of conversion of brain wave signals which are in the frequency range of 10-100Hz.This work provides the baseline for the design of the same modulator using switched capacitor in CMOS technology of 0.18µm TMSC CMOS technology with VDD of 1.8v.The coefficient values a, b, g, c are the ratios of capacitors in switched capacitor level design.

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