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An Integrated Bridgeless PWM Based Power Converter for Power Factor Correction

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***Abstract* - This paper proposes a new integrated bridgeless PWM based power converter for power factor correction. The proposed converter integrates the bridgeless boost rectifier with the asymmetrical pulse-width modulation half-bridge dc–dc converter. The proposed converter provides an isolated dc output voltage without using any full-bridge diode rectifier. Conduction losses are lowered by eliminating the full-bridge diode rectifier. Zero-voltage switching of the power switches reduces the switching power losses. The proposed converter provides high power factor and direct power conversion from the line voltage to an isolated dc output voltage without using the full bridge diode rectifier and also gives a high efficiency, and low cost. Conduction losses are lowered with a simple circuit structure.**

Keywords: **Power converter, Asymmetrical pulse width modulation, Bridgeless, Half bridge, Single stage, Zero- voltage switching (ZVS).**

I. Introduction

The advances in power factor correction (PFC) technology have enabled the development of single-phase ac–dc converters in the recent pieces of literature. The previous single-stage PFC ac–dc converters need the full-bridge diode rectifier. The full-bridge diode rectifier increases the conduction losses and decreases the power efficiency. Especially, at low line voltage, the full-bridge diode rectifier causes high conduction losses, resulting in additional thermal management. These problems can be overcome by eliminating the full-bridge diode rectifier. Up to now, however, any bridgeless single-stage PFC ac–dc converter has not been re- ported for single stage PFC ac–dc converters.

A number of single-stage PFC ac-dc converters have been introduced in the literature. Among them, discontinuous-conduction-mode (DCM) single-stage PFC ac-dc converters are widely used for their simple and efficient structures. Generally, two power stages of the PFC circuit and dc-dc converter are simplified by sharing a common switch or a pair of switches. Most single-stage PFC ac-dc converters use single-switch dc-dc converter topologies such as fly back and forward converters. However, the single-stage single-switch ac-dc converters operate under hard-switching condition.

The voltage stresses of switching devices and power conversion efficiency have not been optimized yet. The practical use of the single-stage single-switch ac-dc converters has been limited for low-power applications with power levels lower than 80 W. Single-stage soft-switching ac-dc converters have been developed to improve the performance of single-stage PFC ac-dc converters. Single-stage soft-switching ac-dc converters based on the half-bridge converter topology are attractive because they provide low component count and zero-voltage switching (ZVS) operation of the power switches. Similar efforts have been put in optimizing and improving the performance of the converter by using active clamping techniques.

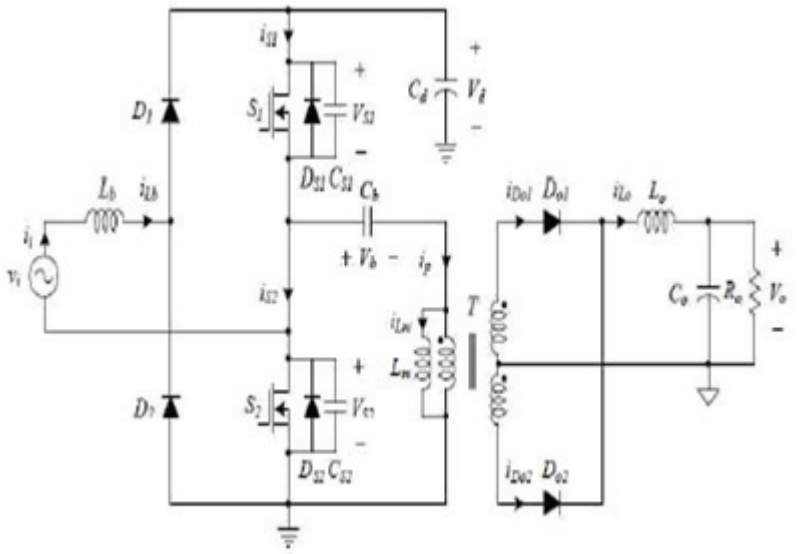

Fig.1 circuit diagram of the proposed converter

II. Circuit Description

Fig.1 shows the circuit diagram f the proposed converter. The bridgeless boost rectifier consists of the boost inductor Lb, dc-link capacitor Cd, and switching devices D, D2, S1, and S2. D1 and D2 are slow-recovery diodes. S1and S2 is metal– oxide–semiconductor field-effect transistors (MOSFETs). DS1 and DS2 are body diodes of S1 and S2, respectively. CS1 and CS2 are the output capacitors of S1 and S2, respectively.

The APWM half-bridge dc–dc converter consists of Cd,,S1, S2 , blocking capacitor Cb, transformer T, output diodes D01 and Do2, output filter inductor Lo, and output filter capacitor Co. Ro is the output resistor. By sharing Cd, S1 and S2, the proposed converter integrates the bridgeless boost rectifier with the APWM half bridge dc–dc converter.

III. Theoretical Analysis

Principle of Operation

For both positive and negative half-line cycle of vi, theproposed converter has symmetric operation. In the positive half-line cycle, S1 is controlled with duty ratio D. Then, the conduction times of the switches S1 and S2 are DTs and (1– D)Ts, respectively. When S1 is turned on, the input current ii flows through Lb, D1, and S1. When S1 is turned off, the input current ii flows through Lb, D1, Cd, S2, and DS2. In the negative half-line cycle, S2 is controlled with duty ratio D. Then, the conduction times of the switches S1 and S2 are (1–D) Ts and DTs, respectively. When S2 is turned on, the input current ii flows through S1, D1, and Lb. When S2 is turned off, the input current ii flows through S1, DS1, Cd, D1, and Lb. The transformer T has the magnetizing inductor Lm and leakage inductor Llk with the turns ratio of 1 : n.

***Interval 1*[t0, t1]:**

At t = t0, S1 is turned on. The input current Ii flows through Lb, D1, and S1. The boost inductor Lb stores energy from the line voltage. The voltage across Lm is Vd – Vb. The primary current ip increases as

$$ilb(t) = vi/Lb(t-to) \qquad (1)$$

Transformer T transfers energy to the output through the output diode Do1. The switch current iS1 is the sum of boost inductor current iLb and the primary current ip.

Interval 2 [t1, t2]

When At t = t1, S1 is turned off. As the primarycurrent ip charges CS1 and discharges CS2, the voltage VS2 across S2 decreases from Vd to zero. Since the time interval in this mode is negligible compared to Ts, the primary current ip and boost inductor current iLb are considered to be constant. When the voltage VS2 across S2 is zero, the primary current ip begins to flow the body diode DS2 of S2.

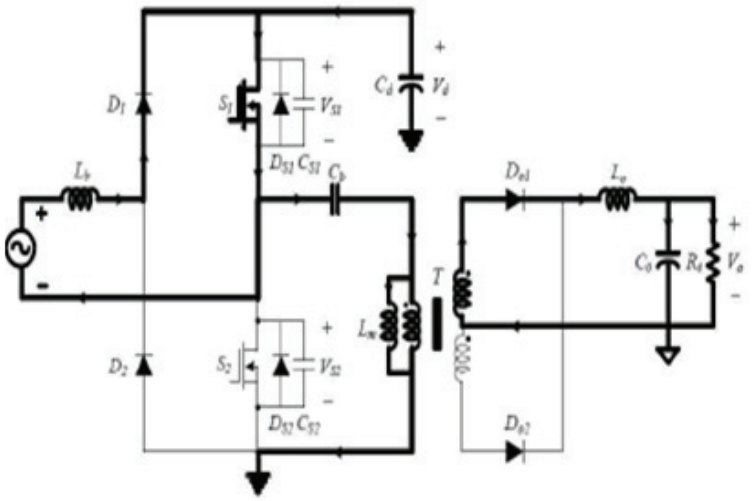

Fig .2 Interval 1 operation

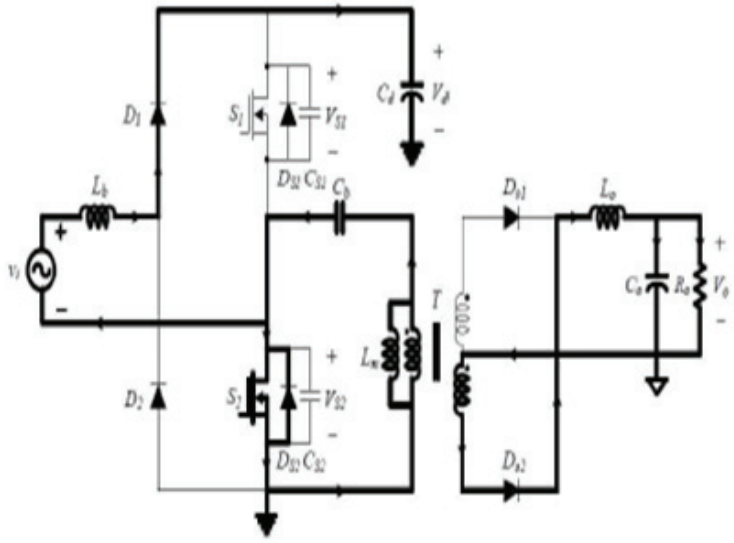

Fig.3 Interval 2

Interval 3 [t2, t3]

At t = t2, S2 is turned on. ZVS of S2 isachieved because the voltage VS2 across S2 is zero. The inputcurrent ii flows through Lb, D1, Cd, S2, and DS2. The energystored in the boost inductor Lb is released to the dc-linkcapacitor Cd. The voltage across Lm is –Vb. The primarycurrent ip decreases as

$$ilb(t) = ilb(t2)-vi/Lb(t-t2) \quad (2)$$

The transformer T transfers energy to the output through the output diode Do2. The switch current iS2 is the sum of boost inductor current iLb and the primary current ip as

Interval 4 [t3, t4]

At t =t3, S2 is turned OFF. As the primary current ip charges CS2 and discharges CS1. The voltage VS1 across S1 decreases from Vd to zero, while the voltage VS2 across S2 increases from zero to Vd. As long as the switch S1 is turned ON before the Magnetizing current iLm changes is direction; ZVS of S1 can be assured. At the secondary side, the output filter inductorcurrent iLo freewheels through both output diodes Do1 and Do2.

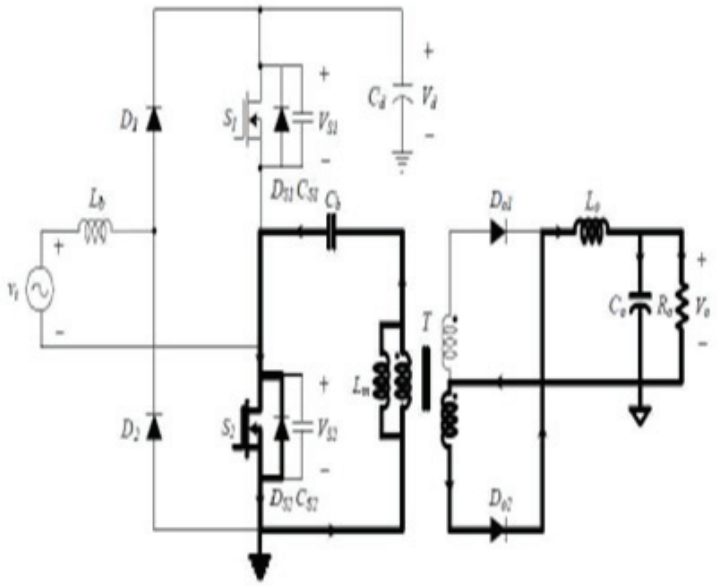

Fig.4 Mode 3 operation

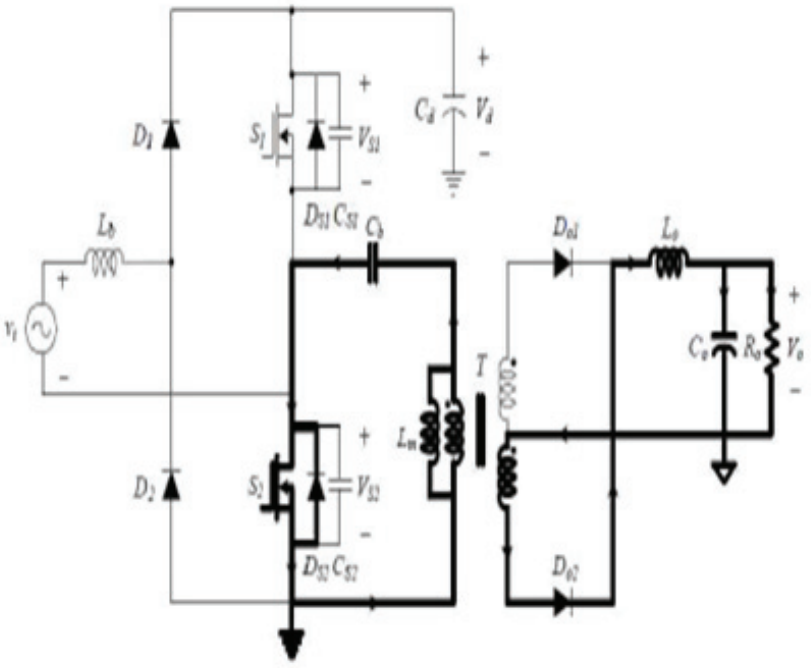

Fig.5 Mode 4 operation

Interval 5 [t4, t5]

At t = t5, the voltage VS1 across S1 is zero.

The primary current ip begins to flow the body diode DS1 of S1. ZVS of S1 can be achieved when S1 is turned on again.

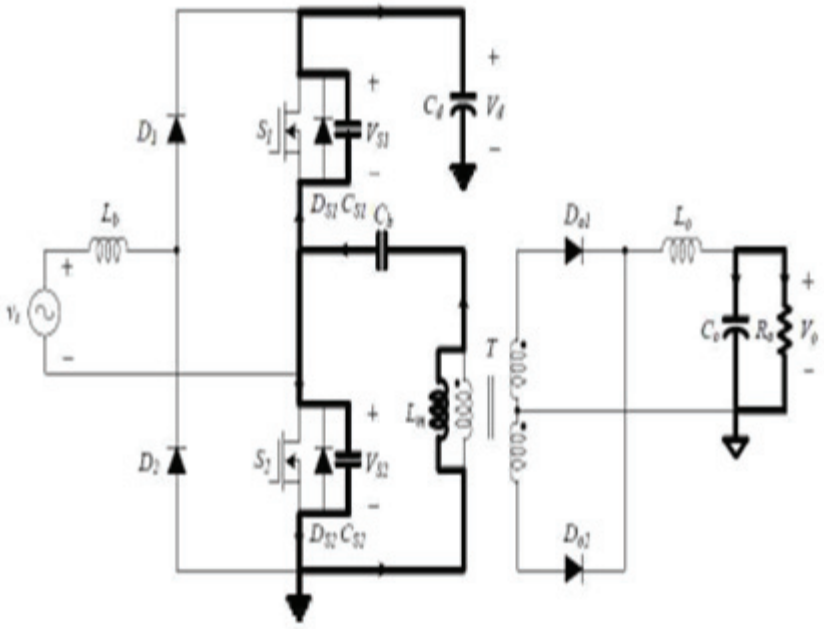

Fig.6 Mode 5 operation

IV. Circuit Analysis

A. Power Factor

The boost inductor Lb operates at DCM. Then, the peak boost inductor current iLb, peak followsthe line voltage vi with a fixed duty ratio to supply the output power for a constant output voltage. Suppose that the converter is lossless and the duty ratio is fixed, the boost inductor Lb should be determined as

$$Lb < Vin$$
$$2DTs/2Pomax. \quad (3)$$

It is defined as the ratio of the real to apparent power. Apparent power is defined as the square root of the sum of the real and reactive power.

B. Efficiency

It is defined as ratio of the output real power to the reactive power.

1. DC Characteristics

From the volt-second balance relation on the magnetizing inductor Lm during Ts, the voltage Vb across the capacitor Cb is expressed as

$$Vb = DVd. \quad (4)$$

From the volt-second balance relation on the output filter inductor Lo during Ts, the following relation between the output voltage Vo and the dc-link capacitor voltage Vd is expressed:

$$Vo/ Vd =2ND (1 - D) \quad (5)$$

V. Simulation and Results

The circuit design was simulated using MATLAB; the schematic circuit is shown in Fig.7 shows the simulation results when the proposed converter supplies 250 W output power.

The proposed bridgeless single-stage ac-dc converter provides high power factor and direct power conversion from the line voltage to an isolated dc output voltage without the suing full-bridge diode rectifier. Fig.8 shows the simulated output of source voltage and current.

When the moment switching pulse is withdrawn, power transfer took place immediately and voltage across the main MOSFET is restored.

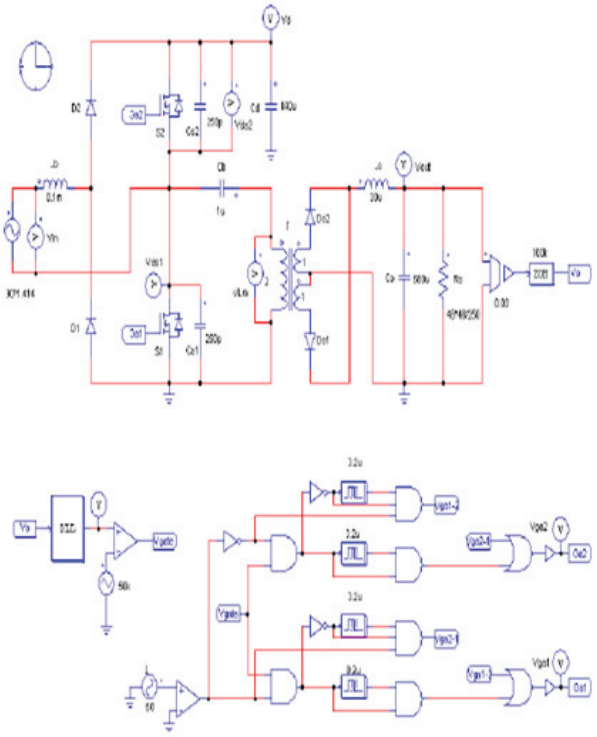

Fig. 7 Simulation diagram

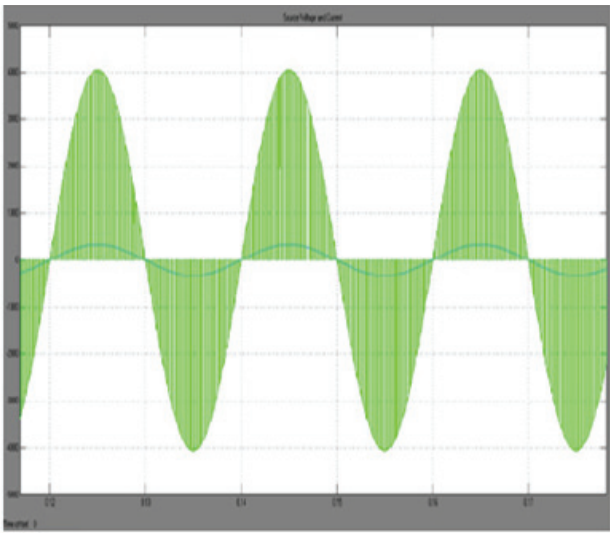

Fig. 8 Source voltage and current

If we properly adjust the delay between turn-off of switch S1 and turn-on of switch S2, we can get ZVS condition for the main switch and auxiliary swich.

The voltage across switch S2 falls before applying the gate pulse. This indicates the ZVS operation of S2. It can be observe that turn-off transition of S2 is capacitance assisted ZVS. Fig. 9 shows the simulated output voltage and current.

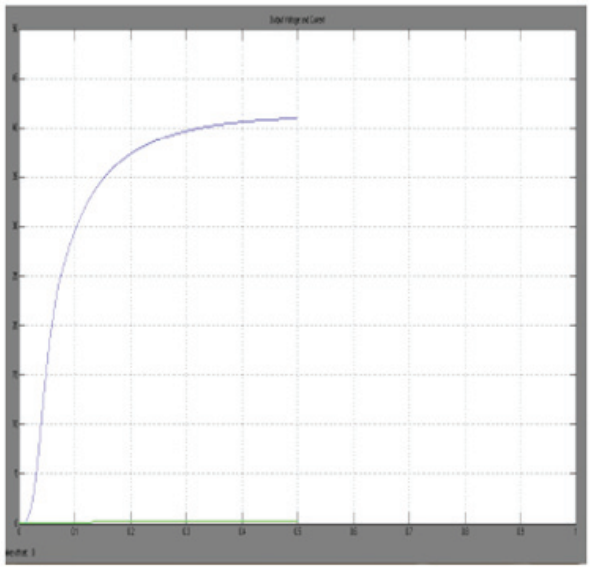

Fig. 9 Output voltage and current

The proposed converter achieves a high-efficiency of 93% with almost unity power factor at 90 Vrms line voltage. Compared to the previous approaches (single-stage design and two-stage design [10]), the proposed approach increase the power efficiency and reduce component counts by lowering conduction losses and by eliminating the full-bridge diode rectifier in the single-stage PFC ac-dc converters. More detailed efficiency comparison, experimental waveforms and circuit design guideline will be discussed in further work.

VI. Conclusion

As a new single-stage PFC scheme, this paper has proposed an integrated bridgeless PWM based power converter. The proposed converter gives a high efficiency by reducing the conduction losses and switching losses.

The proposed converter has the following features for the bridgeless single-stage PFC ac–dc converters:

1. Low switching losses by the ZVS operation of power switches.
2. Simple control method for PFC and output voltage regulation.
3. Low conduction losses by essentially eliminating the full bridge diode rectifier.
4. Reduced component counts by integrating two power conversion.

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